WHAT IS CLAIMED IS:

1. A liquid crystal display (LCD), comprising:

a scan signal line for supplying scanning signals to pixels configuring an LCD panel;

a source signal line for supplying image signals to pixels configuring the LCD panel;

a pixel switch for outputting the image signals to a third electrode from a first electrode connected to the source signal line or stopping the same depending on voltage state of a second electrode connected to the scan signal line;

a power unit for respectively supplying first power and second power to all pixels from outside of a pixel area of the LCD panel;

a control signal line unit respectively including a first control signal line for transmitting a first control signal to all pixels from outside of the pixel area of the LCD panel, and a second control signal line for transmitting a second control signal to all pixels from the outside of the pixel area of the LCD panel;

a liquid crystal unit for transmitting or blocking light according to voltage difference between the image signals and the second power; and

a memory cell unit for receiving the first control signal and the second control signal from the control signal line unit.,

2. The liquid crystal display of claim 1, wherein an operation mode image signal output by the third electrode of the pixel switch is transmitted to the liquid crystal unit, when the first control signal is in low state and the second control signal is in high state, and when the first control signal is in high state, either a still mode image signal

output by the third electrode of the pixel switch or its inveting signal is transmitted to the liquid crystal unit as the second control signal periodically repeats the low and high states according to characteristics of the LCD panel.

3. The LCD of claim 1, wherein the memory cell unit comprises:

a first inverter circuit having an nTFT and a pTFT, a drain electrode of the nTFT being connected to that of the pTFT, and gate electrodes being connected to the third electrode of the pixel switch;

a second inverter circuit having an nTFT and a pTFT, drain electrodes of the nTFT and pTFT being connected to the third electrode of the pixel switch, and gate electrodes being connected to the drain electrodes of the first inverter circuit;

a push nTFT having a drain electrode connected to the first power, a source electrode connected to source electrodes of the pTFTs of the first inverter circuit and the second inverter circuit, and a gate electrode connected to the first control signal line;

a pull nTFT having a source electrode connected to the second power, a drain electrode connected to source electrodes of the nTFTs of the first inverter circuit and the second inverter circuit, and a gate electrode connected to the first control signal line;

an operation nTFT having a gate electrode connected to the second control signal line, and source and drain electrodes connected between the third electrode of the pixel switch and the liquid crystal unit; and

a still pTFT having a gate electrode connected to the second control signal line, and source and drain electrodes connected between the drain electrode of the first

inverter circuit and the liquid crystal unit.

4. The LCD of claim 1, wherein the control signal line unit transmits respective control signals sequentially delayed by a buffer circuit to corresponding pixel areas when the pixel area of the LCD panel is divided into at least two portions either in horizontal direction or, in vertical direction.

5. A low power liquid crystal display (LCD), comprising:

a scan signal line for supplying scanning signals to pixels configuring an LCD panel;

a source signal line for supplying image signals to pixels configuring the LCD panel;

a pixel switch for outputting the image signals to a third electrode from a first electrode connected to the source signal line or stopping the same depending on voltage state of a second electrode connected to the scan signal line;

a power unit for respectively supplying first power, second power and third power to all pixels from outside of a pixel area of the LCD panel;

a control signal line unit respectively including a first control signal line for transmitting a first control signal to all pixels from the outside of the pixel area of the LCD panel, and a second control signal line for transmitting a second control signal to all pixels from outside of the pixel area of the LCD panel;

a liquid crystal unit for transmitting or blocking light according to a difference between the image signals and the third power; and

a level shift unit for receiving the second control signal, lifting the high state by as much as the second power, generating an inverting signal, and outputting the inverting

signal.

6. The liquid crystal display of claim 5, further comprising a memory cell unit.

7. The liquid crystal display of claim 6, wherein the memory cell unit receives the first and second control signals from the control signal line unit and receiving the inverting signal of the second control signal output by the level shift unit,.

8. The liquid crystal display of claim 7, wherein, when the first control signal is in low state and the second control signal is in high state, an operation mode image signal output by a third electrode of the pixel switch is transmitted to the liquid crystal unit, and when the first control signal is in high state, either a still mode image signal output by the third electrode of the pixel switch or its inverting signal is transmitted to the liquid crystal unit as the second control signal periodically repeats the low and high states according to characteristics of the LCD panel.

9. The LCD of claim 7, wherein the memory cell unit comprises:

a first inverter circuit having an nTFT and a pTFT, a drain electrode of the nTFT being connected to that of the pTFT, and gate electrodes being connected to the third electrode of the pixel switch;

a second inverter circuit having an nTFT and a pTFT, drain electrodes of the nTFT and pTFT being connected to the third electrode of the pixel switch, and gate electrodes being connected to the drain electrodes of the first inverter circuit;

a push nTFT having a drain electrode connected to the first power, a source electrode connected to source electrodes of the pTFTs of the first inverter circuit and the second inverter circuit, and a gate electrode connected to the first control signal

line;

a pull nTFT having a source electrode connected to the third power, a drain electrode connected to source electrodes of the nTFTs of the first inverter circuit and the second inverter circuit, and a gate electrode connected to the first control signal line;

an operation nTFT having a gate electrode connected to the second control signal line, and source and drain electrodes connected between the third electrode of the pixel switch and the liquid crystal unit; and

a still nTFT having a gate electrode connected to receive an inverting signal of the second control signal output by the level shift unit, and source and drain electrodes connected between the drain electrode of the first inverter circuit and the liquid crystal unit.

10. The LCD of claim 5, wherein the level shift unit comprises:

a third inverter circuit having an nTFT and a pTFT, a drain electrode of the nTFT being connected to that of the pTFT, gate electrodes being connected to the second control signal line, a source electrode of the pTFT being connected to the second power, and a source electrode of the nTFT being connected to the third power; and

a level-up pTFT having a gate electrode connected to a drain electrode of the third inverter circuit, a source electrode connected to the second power, and a drain electrode connected to the second control signal line.

11. The LCD of claim 5, wherein the control signal line unit transmits respective control signals sequentially delayed by a buffer circuit to corresponding pixel areas when the pixel area of the LCD panel is divided into at least two portions either in

horizontal direction or in vertical direction.

12. In a liquid crystal display (LCD) panel driving method for a pixel switch that receives scanning signals and image signals from scanning signal lines and source signal lines to output the image signals to a memory cell unit that is operated by first and second control signals or stops the image signals to display the same, an LCD driving method comprising:

the memory cell unit transmitting operation mode image signals output by the pixel switch to liquid crystal and displaying the same when the first control signal is in low state and the second control signal is in high state; and

transmitting either a still mode image signal output by a third electrode of the pixel switch or its inverting signal to the liquid crystal as the second control signal periodically repeats low and high states to fit characteristics of an LCD panel when the first control signal is in high state.

13. The method of claim 8, wherein the method further comprises transmitting respective control signals sequentially delayed by a buffer circuit to a corresponding pixel area when the pixel area of the LCD panel is divided into at least two portions in either a horizontal or vertical direction.